TITLE

TRENCH DEVICE STRUCTURE WITH SINGLE-SIDE BURIED STRAP AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a semiconductor memory device, and more particularly, to a deep trench capacitor structure of a volatile memory cell with an improved isolation structure, and method for forming the same.

Description of the Related Art

A typical dynamic random access memory cell (DRAM) is composed of a switching transistor and a coupled storage capacitor. 512MB DRAM is now widely available. There has been still an increased interest in the electronic industry for higher density and higher speed memory cell devices. Research and development efforts are made on an ongoing basis to develop faster and, correspondingly, smaller DRAM devices. Currently, conventional 2D design is gradually being replaced by 3D vertical design in DRAM fabrication. Areas transistors and capacitors occupy on a DRAM cell is greatly reduced by fabricating the capacitor in a deep trench in a semiconductor substrate, thereby minimizing the size of memory cells and power consumption and also increasing operating speeds.

FIG. 1 shows a conventional deep trench structure of a DRAM cell. As shown in FIG. 1, a deep trench (DT) 11

is formed in a p-type semiconductor silicon substrate 10. A deep trench capacitor 12 is then fabricated on the bottom portion of DT 11, which includes a buried plate 14, a node dielectric layer 16 and a storage node 18. The deep trench (DT) 11 can be conventionally formed in the p-type semiconductor substrate 10 by reactive ion etching (RIE). A high-temperature and short-term annealing process using a heavily-doped oxide material (such as arsenic silica glass (ASG)) is then performed. N^+ ions are diffused into the silicon substrate 10 at the lower portion of the deep trench DT 11, thus forming an n^+-type diffusion region 14 to serve as the buried plate of the deep trench capacitor 12. A silicon nitride liner 16 is then formed on the bottom and lower portion sidewall of the trench 11, serving as a node dielectric layer. N-doped polysilicon is deposited into the deep trench 11 and recessed to a predetermined thickness, which serves as storage node 18 of the deep trench capacitor 12.

After a deep trench capacitor 12 is formed in p-type semiconductor substrate 10, a collar insulating layer 20 is formed, lining the sidewall of the deep trench 11 above the deep trench capacitor 12, and recessed to a predetermined depth. Second and third n-doped polysilicon layers 22 and 24 are then deposited onto the deep trench capacitor 12 sequentially. One side of the third polysilicon layer and a portion of the second polysilicon are etched to form shallow trench isolation (STI) structure 26 to isolate two adjacent memory cells. Word lines WL_1 and WL_2, source/drain regions 28, a bit

line contact plug (CB) and a bit line (BL) are fabricated subsequently on/in the p-type silicon substrate 10. With a thermal process, the n-type dopants in the third polysilicon layer 24 diffuse into the contiguous silicon substrate 10 from the side without collar insulating layer 20 to form a buried strap 30 that fuses to source/drain region 28 as a node junction and connects the third and second polysilicon layers 22 and 24 and the deep trench capacitor 12 in the deep trench 11.

However, seams or crystal lattice defects occur when shrinking shallow trench isolation structures, thereby reducing the reliability of memory cells.

SUMMARY OF THE INVENTION

One object of the invention is to provide a deep trench structure with single-side buried strap and a method for fabricating the same, which utilizes collar insulating layer for isolation, thereby reducing memory cell size.

Another object of the invention is to provide a deep trench structure with single-side buried strap, which utilizes collar insulating layer to replace conventional STI structures, thereby simplifying the fabrication.

To achieve these objects, a deep trench device structure and a method for making the same are provided. A deep trench is formed in a semiconductor substrate, and a buried trench capacitor is formed in the lower portion of the deep trench. A collar insulating layer is then formed lining the upper sidewall of the deep trench. A first conductive layer is deposited overlying the buried

trench capacitor in the trench and surrounded by and lower than the collar insulating layer. A portion of the collar insulating layer on the sidewall of the deep trench is then removed to expose a portion of the semiconductor substrate. A second conductive layer is subsequently formed overlying the first conductive layer in the trench, wherein the second conductive layer is lower than the surface of the semiconductor substrate. Finally, a buried strap region is formed by thermal treatment in the semiconductor substrate directly in contact with the second conductive layer without isolation by the collar insulating layer.

A deep trench structure with single-side buried strap is then formed by the above method. One side of the first and second conductive layers in the deep trench is isolated from the semiconductor substrate by the collar insulating layer. The other side of the first conductive layer in the deep trench is still isolated by the collar insulating layer, but a proton of the second conductive layer on the other side of the deep trench directly contacts the semiconductor substrate. Therefore, after a proper thermal treatment, dopants in the second conductive layer can diffuse out to the contiguous semiconductor substrate, thereby forming a single-side buried strap in the semiconductor substrate. A conventional STI structure is replaced by a collar insulating layer.

A detailed description is given in the following, with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIG. 1 shows a conventional deep trench structure of a DRAM cell;

FIG. 2 shows a partial layout of a DRAM array of the invention;

FIGs. 3 to 8 show fabrication of a deep trench device structure with a single-side buried strap along 1-1 direction in FIG. 2 of the invention; and

FIG. 9 is a cross-section showing a DRAM cell with a deep trench device structure with a single-side buried strap along 1-1 direction in FIG. 2, formed as shown in FIGs. 3 to 8;

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a partial layout of a DRAM array of the invention. FIGs. 3 to 8 show fabrication of a deep trench device structure with a single-side buried strap along 1-1 direction in FIG. 2.

In FIG. 3, a pad layer 43, such as a silicon nitride layer, is formed on the surface of a semiconductor silicon substrate 40. Deep trenches (DT hereinafter) 41A and 41B are formed in the silicon substrate 40. Deep trench capacitors 42A and 42B are formed in the lower portion of the deep trenches 41A and 41B respectively by conventional process as described previously. A deep

trench capacitor includes a buried plate 44 in the substrate 40 surrounding the deep trench, a node dielectric layer 46 and a storage node 48. A p-type semiconductor silicon substrate 40 is exemplified hereinafter. Deep trenches (DT) 41A and 41B are formed in the substrate 40 by a patterned pad layer 41 and reactive ion etching (RIE). High-temperature and short-term annealing using a heavily-doped oxide material (such as arsenic silica glass (ASG)) is performed. N-type ions are out-diffused into the p-type semiconductor substrate 40 at the lower portion of the DT 41A and 41B to form n-doped diffusion areas 44 in the substrate 40, serving as buried plates surrounding DT 41A and 41B respectively. Lining layers 46 are then formed on the bottom and sidewalls of DT 41A and 41B respectively. The preferred layer 46 is composed of silicon nitride, oxide-nitride (ON) dual-layers, or oxide-nitride-oxide (ONO) tri-layers, and serves as a node dielectric layer. N-doped polysilicon layers 48 are deposited to fill DT 41A and 41B and then recessed to a predetermined thickness. The exposed dielectric layers 46 on the sidewalls of DT 41A and 42B are also removed, as shown in FIG. 3. The polysilicon layers 48A and 48B serve as storage nodes and the dielectric layers 46 interposed between the polysilicon layers 48A and 48B and the n-type diffusion areas 44 serve as node dielectric layers of the deep trench capacitor 42A and 42B respectively.

In FIG. 4, collar insulating layers 50A and 50B are formed on sidewall of DT 41A and 41B above the deep trench capacitors 42A and 42B respectively. The exposed

sidewalls of DT 41A and 41B are oxidized to form silicon oxide layers. An oxide layer, such as tetra ethyle ortho silicate (TEOS), is deposited by chemical vapor deposition (CVD), conformally on the surface of the pad layer 43 and the inner surface of DT 41A and 41B at a thickness of 200 to 300Å. The oxide layer on the surface of pad layer 43 and on the top of the deep trench capacitors 42A and 42B are removed by anisotropic dry etching, thereby forming collar insulating layers 50A and 50B on the sidewalls of DT 41A and 41B above deep trench capacitors 42A and 42B respectively, as shown in FIG. 4.

An n-type doped second polysilicon layer is deposited on the substrate 40 and fills DT 41A and 41B. Excess n-type doped polysilicon layer on the pad layer 43 is removed by chemical mechanical polishing (CMP). The n-type doped polysilicon in DT 41A and 41B are then recessed to a predetermined depth below the surface of the p-type substrate 40 as polysilicon layers 52A and 52B, as FIG. 4 shows.

In FIG. 5, a lining layer 53 and an undoped polysilicon or amorphous silicon layer 55 are deposited conformally on the surface of the pad layer 43 and the DT 41A and 41B. Preferably, the lining layer 53 is a silicon nitride layer at a thickness of about 100Å formed by low pressure chemical vapor deposition (LPCVD). An undoped polysilicon or amorphous silicon layer 55 is then deposited by LPCVD on the surface of the lining layer 53 at a thickness of about 50 to 100Å. As FIG. 5 shows, the lining layer 53 and the undoped polysilicon or amorphous silicon layer 55 conformally cover the collar insulating

layers 50A and 50B and the underlying polysilicon conductive layers 52A and 52B.

As further shown in FIG. 5, tilt ion implantation is performed on the undoped polysilicon or amorphous silicon layer 55 at a preferred tilt implant angle of 7° to 15°, implantation energy from 5 to 20 KeV, and with implantation dosage of 1×10^{14} to 1×10^{15} ions/cm^2. The preferred dopant is BF_2 or B. Due to the high aspect ratio of DT 41A and 41B, a portion of the undoped polysilicon or amorphous silicon layer 55 on the DT 41A and 41B and on the top surface of the polysilicon conductive layers 52A and 52B will be shielded and not implanted, as shown in FIG, 5. Meanwhile, the silicon nitride lining layer 53 can prevent the underlying collar insulating layers 50A and 50B from implantation and serve as a hard mask in the subsequent process.

In FIG. 6, the unimplanted undoped polysilicon or amorphous silicon layer 55 is removed by selective wet etching to expose the underlying lining layer 53, with different etching rates for each. In a preferred embodiment, when BF_2 or B is utilized as dopant, low concentration ammonium solution is used as the selective wet etching solution. The etching rate of low concentration ammonium solution to the unimplanted n-doped polysilicon or amorphous silicon layer is much higher than that implanted. Thus, the unimplanted undoped polysilicon or amorphous silicon layer is etched to expose the underlying lining layer 53.

The exposed lining layer 53 is then etched with the remaining implanted undoped polysilicon or amorphous

silicon layer 55 as a mask to expose collar insulating layers 50A and 50B on one sidewall of DT 41A and 41B. The exposed collar insulating layers 50A and 50B are subsequently removed with the remaining implanted undoped polysilicon or amorphous silicon layer 55 and the lining layer 53 as a mask to form lower collar insulating layers 50A' and 50B' on one sidewall of DT 41A and 41B respectively, as FIG. 7 shows. The remaining implanted undoped polysilicon or amorphous silicon layer 55 and the lining layer 53 are then removed, thereby forming DT 41A and 41B with high collar insulating layers 50A and 50B on one sidewall and lower collar insulating layers 50A' and 50B' of the opposite sidewall.

In FIG. 8, a third n-type doped polysilicon layer is deposited on DT 41A and 41B. The excess polysilicon layer on the pad layer 43 is removed by CMP. The polysilicon layers 54A and 54B in DT 41A and 41B respectively are recessed to below a predetermined surface of the substrate 40. As shown in FIG. 8, one side of polysilicon layers 54A and 54B is isolated by higher collar insulating layer 50A and 50B from the substrate 10. However, since the collar insulating layers 50A' and 50B' are lower than the polysilicon layers 54A and 54B on the opposite side, a portion of the polysilicon layers 54A and 54B directly contact the substrate 40. With an extra thermal treatment or in the subsequent thermal process, the n-type dopants in the polysilicon layers 54A and 54B will diffuse out to the p-type silicon substrate 40 without the barrier of the collar insulating layers 50A' and 50B', thereby forming

single-side buried strap regions 60A and 60B in the substrate 40 adjacent to DT 41A and 41B respectively. The pad layer 43 is planarized after deep trench devices are formed.

FIG. 9 is a cross-section showing a DRAM cell with a deep trench device structure with a single-side buried strap along 1-1 direction in FIG. 2, formed by the above process. After deep trench device structures with single-side buried straps are formed, a gate electrode (GC), source/drain regions 58 and a bit line contact plug (BC) are formed on the surface of the semiconductor silicon substrate 40 by conventional process. As shown in FIG. 9, the single-side buried strap 60B diffuses out to contact the source/drain region 58 of the transistor, serving as a node junction to connect the polysilicon layer 54B, 52B and the underlying deep trench capacitor 42B in DT 41B. The DT 41B is isolated from the adjacent transistor by a higher collar insulating layer 50B, thereby omitting a conventional STI structure.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.